In the Title:

Please replace the title with:

METHOD OF FORMING A LOW VOLTAGE GATE OXIDE LAYER AND TUNNEL OXIDE LAYER IN AN EEPROM CELL

In the Specification:

In the Abstract

Please replace the Abstract text with the text below:

A method of fabricating a non-volatile memory embedded logic circuit having a low voltage logic gate oxide layer and tunnel oxide layer is described. Both the low voltage logic gate oxide and the tunnel oxide layers are formed in a single step, thereby reducing the number of overall processing steps needed to form the devices.

In the Description of the Invention

In the specification, please replace the two paragraphs of text beginning on page 5, line 17 to page 6, line 30, with the text below. The text below includes additional paragraph breaks, a rearrangement of some sentences, and rephrased text to better match the referenced figures and improve overall clarity. Also, corresponding references to the first, second, and third device areas as listed in claim 1 have been added. No new matter has been added.

In step (i), a pad oxide layer 44 is formed above a semiconductor substrate 46. A nitride layer 42 is deposited on top of the pad oxide layer 44. Next, a patterned photoresist layer 40 is formed above the nitride layer 42. The nitride layer 42, pad oxide layer 44, and substrate 46 are etched, so as to produce an exposed area 50 where an isolation structure is to be formed.

The isolation structure surrounds and electrically isolates individual device areas in which logic cells and embedded memory cells are built. Though the isolation structure shown in subsequent figures is of the Shallow Trench

Isolation (STI) type, it is also possible to use other isolation methods such as Local Oxidation of Silicon (LOCOS). In an STI process, the isolation structure is formed by etching a shallow trench through a nitride layer 42 and pad oxide 44 and into an exposed substrate area, for example to a depth of about 4000 Å, and then filled or thermally grown, for example with silicon dioxide, using a deposition or growth process according to methods known to one skilled in the art. In step (ii), a shallow trench 48 is formed by an etch of the exposed area 50, followed by an oxide fill step that fills the shallow trench with, for example, silicon dioxide. A subsequent planarization process, using the nitride layer 42 as a natural stop, removes or polishes off any excess silicon dioxide material, forming a leveled oxide plateau 49 on top of the STI structure 48. As an example, the polishing step may be a chemical mechanical planarization (CMP) process.

In step (iii), the nitride layer 42 and the pad oxide layer 44 are sequentially removed to form an STI isolation structure 48 shown. The STI isolation structure is formed to electrically separate adjacent device areas. A variety of adjacent and non-adjacent device structures may now be formed.

Next, as shown in Figures 3A and B at step (iv), a high voltage (HV) gate oxide layer 68, for example having an approximate 250 Å thickness, is formed over the substrate 46. The oxide layer 68 is masked with a patterned photoresist. The exposed part of the oxide layer 68 is then etched to reveal portions of the underlying substrate 46 as shown in step (v). Next, in exposed areas 52, 54, a second or subsequent, thinner oxide layer will be formed. The formation of the first or second oxide layer may be carried out by thermal oxidation of the substrate, chemical vapor deposition, or atomic layer deposition. As shown in step (vi), a first device area will be used to form an EEPROM tunnel oxide layer 58, a second device area will be used to form a high voltage

logic gate oxide layer 56, and a third device area will be used to form a low voltage logic gate oxide layer 67. Referring to Figure 2B, an N+ region may be developed in the EEPROM cell area to form a control gate 80. The HV gate oxide layer 56 and the tunnel oxide layer 58 each, for example, approximately 70 Å thick, have been formed on the exposed portions 52, 54 of the substrate 46. This layer of thin gate oxide 56, 58 serves as a gate oxide 56 for the low voltage (LV) logic gate and a tunnel oxide 58 for the EEPROM cell respectively. The low voltage logic gate oxide layer 56 may have essentially the same thickness as the tunnel oxide layer 55.

Thereafter, as shown in Figure (vii), a polysilicon layer 64, 66 is deposited on top of the oxide layers 56, 58, 67, and 68 to form a control gate layer 64 over the gate oxide layer 56 in the logic gate area and a floating gate layer 66 over the tunnel oxide layer 58 in the EEPROM cell area respectively.